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Design and Preliminary Evaluation of CMOS Image Sensor with Pseudorandom Pixel Placement

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1 Introduction

The ultimate purpose of the image sensor is to obtain the clear image, especially the clear image we see. However, the jaggy which appears at the edge of the object in the image, which is composed of some pair of pixels, and it becomes the serious factor to defect the clearness of the image, since our eye severely perceives such jaggy, and it cannot be intrinsically eliminated by increased number of pixels.

The authors has proposed the image sensor whose pixels are pseudorandomly arranged in order to decrease the jaggy effect[1, 2]. In this paper, we describe the design and preliminary evaluation of CMOS image sensor with pseudorandom pixel placement.

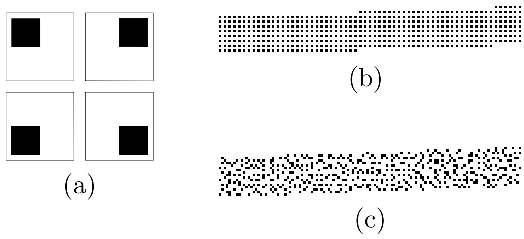


Figure 1: Four types of pixels(a) and the representaions of a slant line using (b)the lattice and (c)the pseudorandom pixel placements, repsectively.

2 Pixel configuration for pseudorandom pixel placement

Figure 1 shows the model of the pixels for pseudorandom arrangement, where white and black squares are the pixel boundary and photo receptor area, respectively. There four types of pixels where the position of photo receptor are different, while the circuit and the electrical connections are identical. The arrangement of one of the pixels forms the conventional image sensor as shown in Fig.1(b), while the arrangement of pseudorandomly selected pixels, the pixel selection is determined by the pseudorandom number, forms the pseudorandom arrangement of photo receptors as shown in Fig.1(c). The jaggy appears at the edge of the slant line for the conventional lattice placement in Fig.1(b), while the jaggy is diffused out to small roughness of the boundary for the pseudorandom placement in Fig.1(c). Our eye perceive the jaggy in lattice placement, one step in the almost horizontal line more severely by Vernier Acuity of the eye than the random roughness even if the size of step or roughness are equal[4].

3 CMOS image sensor with pseudorandom pixel placement

Figure 2(a) shows the circuit architecture of the designed CMOS image sensor with pseudorandom pixel placement, which is simple CMOS image sensor with 3Tr-APS pixel. Figure 2(b) shows the designed layout of four pixels, where the positions of the photo diodes are different, with identical circuit and positions of electrodes; power, reset, row select, and column data. The sizes of the pixel and photo diode are 10μm square and 5μm square, respectively.

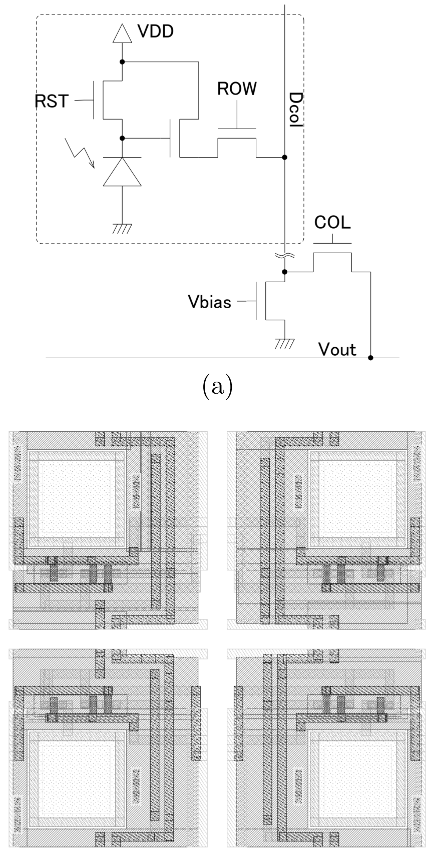
Two types of pixel plain, the conventional lattice placement and the pseudorandom placement are designed, whose numbers of pixels are both 128×64. The whole CMOS image sensor of 128×128 pixels is designed with two pixel plains, row decoder, column decoder & buffer, and output buffer.

Figure 3(a) shows the fabricated CMOS image sensor with two types of pixel plain[1], and the magnified lattice and pseudorandom pixel plains are shown in Fig.3(b) and Fig.3(c), respectively. The measured specifications of the fabricated CMOS image sensor are summarized in Tab.1.

The captured images for the object of 'A' shape by both pixel plains are shown in Fig.4, where the images are shown by one 'active' pixel in 2×2 pixels unit, whose position is identical for that in designed CMOS image sensor. (The optimum parameters of the display, displacement in pixel and fill factor, will be discussed in our future work.)

The different size jaggies appear in the captured images by the conventional lattice placement as shown in Fig.4(a) and Fig.4(b) for different angle of the object, while the small roughness in the captured images by the conventional lattice placement in Fig.4(c) and Fig.4(d) have small dependency on the angle of the object, and this roughness can be reduced by the decreased size of pixels.

[1]The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.



(a)

(b)

Figure 2: Circuit architecture of the designed CMOS image sensor(a) and four types of the pixel circuit layouts(b).

Table 1: Specifications of the fabricated CMOS image sensor.

Process	Standard CMOS 0.18μm, 5M1P
Number of Pixel	128×128 (128×64: Lattice) (128×64: Pseudorandom)
Pixel Size	10[μm] × 10[μm]
Photo Diode	Psub-Nwell
Fill Factor	25[%]
Supply Voltage	3.3[V]
Conversion Efficiencyη	64[μV/e^-]
Sensitivity	6.93 [V/s·lx]

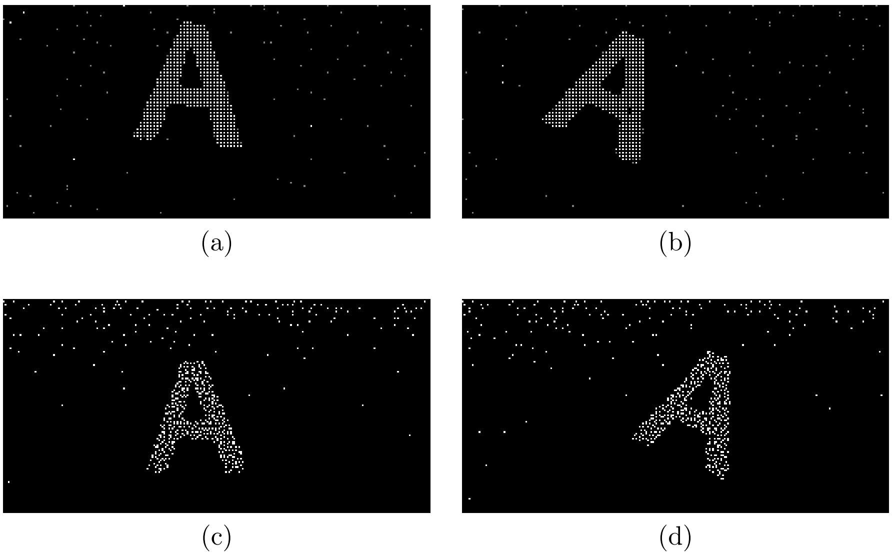
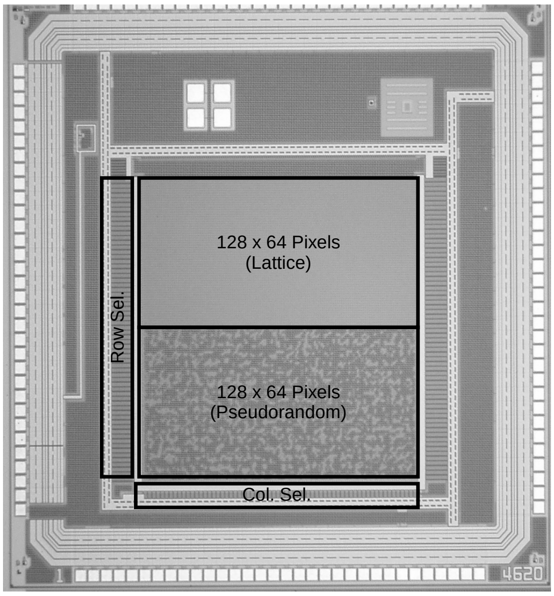
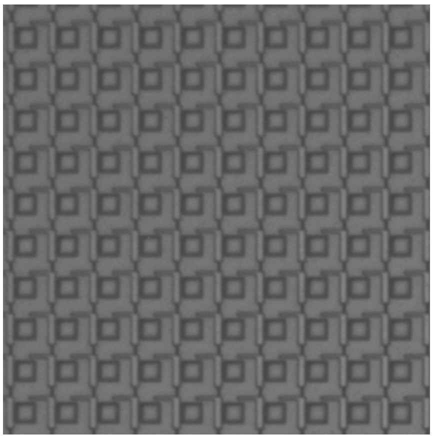


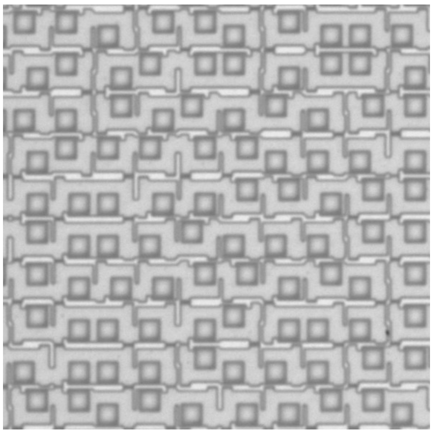
Figure 4: Captured images by the lattice(a)(b) and the pseudorandom(c)(d) pixels area.



(a)



(b)



(c)

Figure 3: Photograph of the fabricated CMOS image sensor(a) and the manified photograph for (b)the lattice and (c)the pseudorandom pixel areas, respectively.

4 Conclusion

In this paper, the design of the CMOS image sensor with pseudorandom pixel placement is described with the comparison of the conventional pixel placement, as well as their preliminary evaluation.

References

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